

WHAT IS CLAIMED IS:

1 1. An adaptive computing integrated circuit configurable to perform a
2 plurality of functions, comprising:
3 a plurality of heterogeneous computational elements; and
4 an interconnection network coupled to the plurality of heterogeneous
5 computational elements, the interconnection network operative to configure the plurality of
6 heterogeneous computational elements;
7 wherein a first group of heterogeneous computational elements is configurable
8 to form a first functional unit to implement a first function;
9 wherein a second group of heterogeneous computational elements is
10 configurable to form a second functional unit to implement a second function; and
11 wherein if the second function is not currently used, one or more of the second
12 group of heterogeneous computational elements are reconfigurable by the interconnection
13 network to implement the first function.

1 2. The adaptive computing integrated circuit of claim 1 wherein if the
2 second function is not currently used, the one or more of the second group of heterogeneous
3 computational elements are reconfigurable to implement the first function by forming one or
4 more additional instances of the first functional unit.

1 3 . The adaptive computing integrated circuit of claim 1 wherein if the
2 second function is not currently used, one or more of the first group of heterogeneous
3 computational elements and the one or more of the second group of heterogeneous
4 computational elements are reconfigurable to form a single functional unit to implement the
5 first function.

1 4. The adaptive computing integrated circuit of claim 1 wherein if the
2 second function is not currently used, the one or more of the second group of heterogeneous
3 computational elements are reconfigurable by the interconnection network to implement one
4 or more of the plurality of functions other than the second function.

1 5. The adaptive computing integrated circuit of claim 1 wherein if a third
2 function is to be implemented, one or more of the first group of heterogeneous computational
3 elements and/or the one or more of the second group of heterogeneous computational
4 elements are reconfigurable by the interconnection network to implement the third function.

1 6. An adaptive computing integrated circuit, comprising:
2 a plurality of reconfigurable matrices, the plurality of reconfigurable matrices
3 including a plurality of heterogeneous computational units, each heterogeneous
4 computational unit having a plurality of fixed computational elements, the plurality of fixed
5 computational elements including a first computational element having a first architecture
6 and a second computational element having a second architecture, the first architecture
7 distinct from the second architecture, the plurality of heterogeneous computational units
8 coupled to an interconnect network and reconfigurable in response to configuration
9 information; and

10 a matrix interconnection network coupled to the plurality of reconfigurable
11 matrices, the matrix interconnection network operative to reconfigure the plurality of
12 reconfigurable matrices in response to the configuration information for a plurality of
13 operating modes;

14 wherein a first group of heterogeneous computational units is reconfigurable
15 to form a first functional unit to implement a first operating mode;

16 wherein a second group of heterogeneous computational units is
17 reconfigurable to form a second functional unit to implement a second operating mode;

18 wherein if the second operating mode is not currently used, one or more of the
19 second group of heterogeneous computational units are reconfigurable to implement the first
20 operating mode.

1 7. The adaptive computing integrated circuit of claim 6 wherein if the
2 second operating mode is not currently used, the one or more of the second group of
3 heterogeneous computational units are reconfigurable to implement the first operating mode
4 by forming one or more additional instances of the first functional unit.

1 8. The adaptive computing integrated circuit of claim 6 wherein if the
2 second operating mode is not currently used, one or more of the first group of heterogeneous
3 computational units and the one or more of the second group of heterogeneous computational
4 units are reconfigurable to form a single functional unit to implement the first operating
5 mode.

1 9. The adaptive computing integrated circuit of claim 6 wherein if the
2 second operating mode is not currently used, the one or more of the second group of

3 heterogeneous computational units are reconfigurable to implement one or more of the
4 plurality of operating modes other than the second operating mode.

1 10. The adaptive computing integrated circuit of claim 6 wherein if a third
2 operating mode is to be implemented, one or more of the first group of heterogeneous
3 computational units and/or the one or more of the second group of heterogeneous
4 computational units are reconfigurable to implement the third operating mode.

1 11. An adaptive computing integrated circuit, comprising:
2 a plurality of heterogeneous computational elements, the plurality of
3 heterogeneous computational elements including a first computational element and a second
4 computational element, the first computational element having a first fixed architecture of a
5 plurality of fixed architecture and the second computational element having a second fixed
6 architecture of the plurality of fixed architectures, the first fixed architecture being different
7 than the second fixed architecture, and the plurality of fixed architectures including functions
8 for memory, addition, multiplication, complex multiplication, subtraction, configuration,
9 reconfiguration, control, input, output, and field programmability; and

10 an interconnection network coupled to the plurality of heterogeneous
11 computational elements, the interconnection network operative to configure the plurality of
12 heterogeneous computational elements;

13 wherein a first group of heterogeneous computational elements is
14 reconfigurable to form a first functional unit to implement a first function;

15 wherein a second group of heterogeneous computational elements is
16 reconfigurable to form a second functional unit to implement a second function; and

17 wherein if the second function is not currently used, one or more of the second
18 group of heterogeneous computational elements are reconfigurable by the interconnection
19 network to implement the first function.

1 12. The adaptive computing integrated circuit of claim 11 wherein if the
2 second function is not currently used, the one or more of the second group of heterogeneous
3 computational elements are reconfigurable to implement the first function by forming one or
4 more additional instances of the first functional unit.

1 13 . The adaptive computing integrated circuit of claim 11 wherein if the
2 second function is not currently used, one or more of the first group of heterogeneous

3 computational elements and the one or more of the second group of heterogeneous
4 computational elements are reconfigurable to form a single functional unit to implement the
5 first function.

1 14. The adaptive computing integrated circuit of claim 11 wherein if the
2 second function is not currently used, the one or more of the second group of heterogeneous
3 computational elements are reconfigurable by the interconnection network to implement one
4 or more of the plurality of functions other than the second function.

1 15. The adaptive computing integrated circuit of claim 11 wherein if a
2 third function is to be implemented, one or more of the first group of heterogeneous
3 computational elements and/or the one or more of the second group of heterogeneous
4 computational elements are reconfigurable by the interconnection network to implement the
5 third function.

16 . An adaptive computing integrated circuit, comprising:

1 a plurality of heterogeneous computational elements, the plurality of

2 heterogeneous computational elements including a first computational element and a second
3 computational element, the first computational element having a first fixed architecture and
4 the second computational element having a second fixed architecture, the first fixed
5 architecture being different than the second fixed architecture; and

6 an interconnection network coupled to the plurality of heterogeneous

7 computational elements, the interconnection network operative to configure a first group of
8 heterogeneous computational elements to form a first functional unit for a first functional
9 mode of a plurality of functional modes, in response to first configuration information, and
10 the interconnection network further operative to reconfigure a second group of heterogeneous
11 computational elements to form a second functional unit for a second functional mode of the
12 plurality of functional modes, in response to second configuration information, the first
13 functional mode being different than the second functional mode, and the plurality of
14 functional modes including linear algorithmic operations, non-linear algorithmic operations,
15 finite state machine operations, memory operations, and bit-level manipulations;

16 wherein if the second functional mode is not currently used, one or more of

17 the second group of heterogeneous computational units are reconfigurable to implement the
18 first functional mode.

1 17. The adaptive computing integrated circuit of claim 16 wherein if the
2 second functional mode is not currently used, the one or more of the second group of
3 heterogeneous computational elements are reconfigurable to implement the first functional
4 mode by forming one or more additional instances of the first functional unit.

1 18. The adaptive computing integrated circuit of claim 16 wherein if the
2 second functional mode is not currently used, one or more of the first group of heterogeneous
3 computational elements and the one or more of the second group of heterogeneous
4 computational elements are reconfigurable to form a single functional unit to implement the
5 first functional mode.

1 19. The adaptive computing integrated circuit of claim 16 wherein if the
2 second functional mode is not currently used, the one or more of the second group of
3 heterogeneous computational elements are reconfigurable by the interconnection network to
4 implement one or more of the plurality of functional modes other than the second functional
5 mode.

1 20. The adaptive computing integrated circuit of claim 16 wherein if a
2 third functional mode is to be implemented, one or more of the first group of heterogeneous
3 computational elements and/or the one or more of the second group of heterogeneous
4 computational elements are reconfigurable by the interconnection network to implement the
5 third functional mode.

1 21. A method for allocating hardware resources within an adaptive
2 computing integrated circuit, comprising:

3 in response to first configuration information, configuring a first group of
4 heterogeneous computational elements to form a first functional unit to implement a first
5 function and configuring a second group of heterogeneous computational elements to form a
6 second functional unit to implement a second function; and

7 in response to second configuration information, reconfiguring one or more of
8 the second group of heterogeneous computational elements to implement the first function.

1 22. The method of claim 21 wherein the second configuration information
2 is generated when the second function is not currently used.

1 23. The method of claim 21 wherein in response to the second
2 configuration information, the one or more of the second group of heterogeneous
3 computational elements are reconfigured to form one or more additional instances of the first
4 functional unit to implement the first function.

1 24 . The method of claim 21 wherein in response to the second
2 configuration information, one or more of the first group of heterogeneous computational
3 elements and the one or more of the second group of heterogeneous computational elements
4 are reconfigured to form a single functional unit to implement the first function.

1 25. The method of claim 21 further comprising:
2 in response to third configuration information, reconfiguring one or more of
3 the first group of heterogeneous computational elements and/or the one or more of the second
4 group of heterogeneous computational elements to implement a third function.